MICROCONTROLLER/PROCESSOR

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M8052

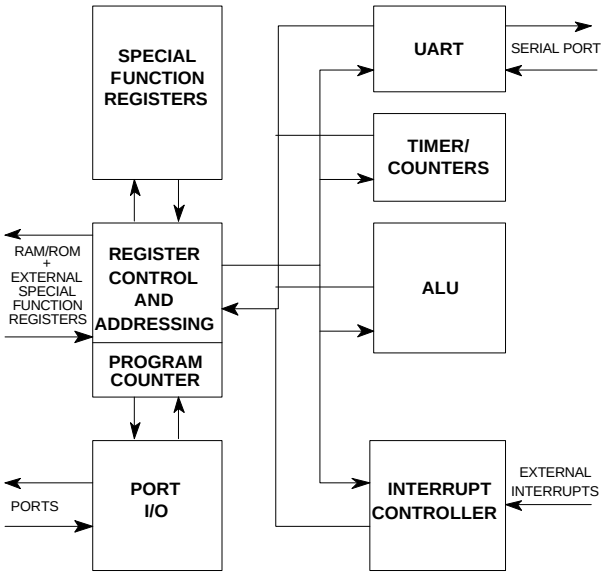
8-BIT MICROCONTROLLER

OVERVIEW

The M8052 is a high performance 8-bit microcontroller.

This microcode-free design is software compatible (including instruction execution times) with the industry standard 8052AH and 8752BH discrete devices, having all their core features, plus the additional features corresponding to standard 8052/8032/80C52BH/80C32BH/87C52 parts except that ONCE mode and Program Lock are not supported.

BLOCK DIAGRAM



KEY FEATURES

- Software compatible with the Intel 8052, 8032, 80C52, 80C53 and 87C52
- Up to 64K bytes of external Data Memory
- Up to 256 bytes of internal Data Memory
- Up to 64K bytes of RAM or ROM Program Memory
- Memory Download mode
- Three 16-bit timer/counters
- Full-duplex serial port
- Power-saving modes
- Support for External SFRs
- Fully synthesizable
- Scan test ready

DELIVERABLES

- Verilog source code
- VHDL source code
- Synthesis script for Design Compiler
- Verilog & VHDL test benches
- Reference technology netlist

RELATED PRODUCT

- M8051 microcontroller

SOFT CORES

DESIGN FEATURES

SERIAL PORT AND TIMER/COUNTERS: These are important features of both the original device and the M8052, simplifying the system design required for a range of possible applications.

The serial port is both full duplex and receive buffered. In addition, the baud rates for transmission and reception can be taken from separate timers, allowing data to be sent and received simultaneously at different cps rates.

DATA & PROGRAM MEMORY: The M8052 can address internal Data Memory of up to 256 bytes and internal Program RAM or ROM of up to 64K bytes via the function interconnect signals.

It can also address up to 64K bytes of external Data RAM, and 64K bytes of external Program ROM via the I/O ports.

PROGRAM MEMORY DOWNLOAD (DLM) MODE: Program Memory may be implemented in RAM, and read/write access to this memory is provided so that it may be "downloaded" from the Master CPU.

MEMORY SIZE REGISTER: The function of this register is to allow a configurable internal memory size for the device. The minimum allowed is 256 bytes, the maximum is 64K bytes.

EXTERNAL SPECIAL FUNCTION REGISTERS: Up to 106 external special function registers (ESFRs) may be added to the M8052 core.

ESFRs are memory mapped into Direct Memory between addresses 80 hex and FF hex in the same manner as core SFRs and may occupy any address that is not occupied by a core SFR.

POWER-SAVING MODES

The M8052 has two “power-saving” modes: Idle mode and Power Down mode. In Idle mode, the clock to the CPU is stopped but the timer/counters and the serial port are still active. In Power Down mode, the clock to the entire M8052 is stopped.

REFERENCE TECHNOLOGY GATE COUNT: 10500

SIGNAL DESCRIPTION

The M8052 has 163 external signals; 55 inputs and 108 outputs.

PROCESSOR INPUTS		
SIGNAL	**TYPE**	**DESCRIPTION**
NEA	Input	Not External Access, enables the program counter value onto Port 0 and Port 2 pins
NX1	Input	Clock Input from oscillator (1 Instruction cycle is 12 clock cycles long)
NX2	Input	Clock Input from oscillator, stoppable in Idle mode
AI[7:0]	Input	Input Port 0 Data bits 7 to 0
BI[7:0]	Input	Input Port 1 Data bits 7 to 0
CI[7:0]	Input	Input Port 2 Data bits 7 to 0
DI[7:0]	Input	Input Port 3 Data bits 7 to 0
RST	Input	Used to reset status flags and set PC to zero
ALEI	Input	ALE input, used to select Download Mode
PSEI	Input	PSEN input, used to select Download Mode
PROCESSOR OUTPUTS		
OA[7:0]	Output	Output Port 0 Data bits 7 to 0
OB[7:0]	Output	Output Port 1 Data bits 7 to 0
OC[7:0]	Output	Output Port 2 Data bits 7 to 0
OD[7:0]	Output	Output Port 3 Data bits 7 to 0
AE[7:0]	Output	Bidirectional control lines for port 0 Data
BE[7:0]	Output	Bidirectional control lines for port 1 Data
CE[7:0]	Output	Bidirectional control lines for port 2 Data
DE[7:0]	Output	Bidirectional control lines for port 3 Data
ALE	Output	Address Latch Enable
NPSEN	Output	External Program Memory Enable
NALEN	Output	Bidirect control line for ALE and PSEN
XOFF	Output	Oscillator disable signal. Used in Power Down mode to stop the device oscillator
IDLE	Output	Idle mode clock qualifier. Used externally in Idle mode to stop the NX2 clock input to the core
FUNCTIONAL INTERCONNECT SIGNALS		
M[15:0]	Output	Program Memory Address lines
MD[7:0]	Input	Program Memory Data Bus
NMOE	Output	Program Memory Output Enable, active low
NMWE	Output	Program Memory Write Strobe, active low
DLM	Output	Download mode, for loading Program Memory
FA[7:0]	Output	Register File Address lines
FO[7:0]	Output	Register File Data Outputs
FI[7:0]	Input	Register File Data Inputs
NFOE	Output	Register File Output Enable, active low
NFWE	Output	Register File Write Strobe, active low
NSFROE	Output	External SFR Output Enable, active low
NSFRWE	Output	External SFR Write Strobe, active low
NESFR	Input	Not External SFR Acknowledge, active low

The functional interconnect signals allow the end user to choose the appropriate memory blocks for each implementation and to configure internal Program memory as downloadable RAM if required.

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